



# Low-Side MOSFET Drivers Application and Lab Evaluation

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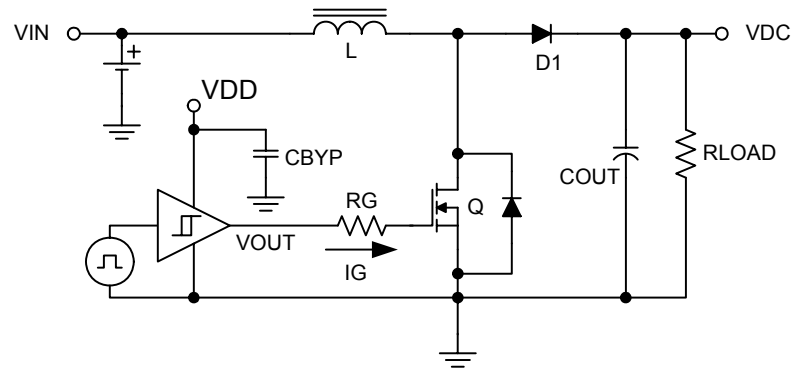
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- Overview of low-side driver applications
  - Clamped Inductive switching
  - Synchronous rectifier switching
  - Transformer drive applications
- Discrete and integrated driver solutions
- Driver datasheet current ratings
- Techniques for evaluating driver current capability in the lab

# When are External Drivers Needed?

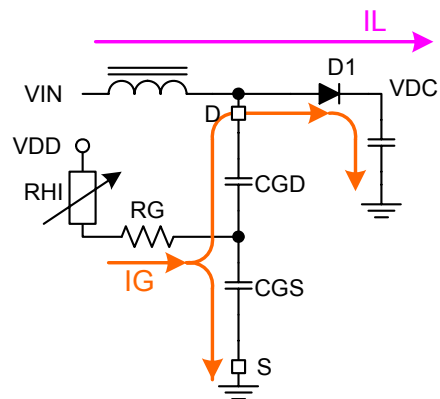
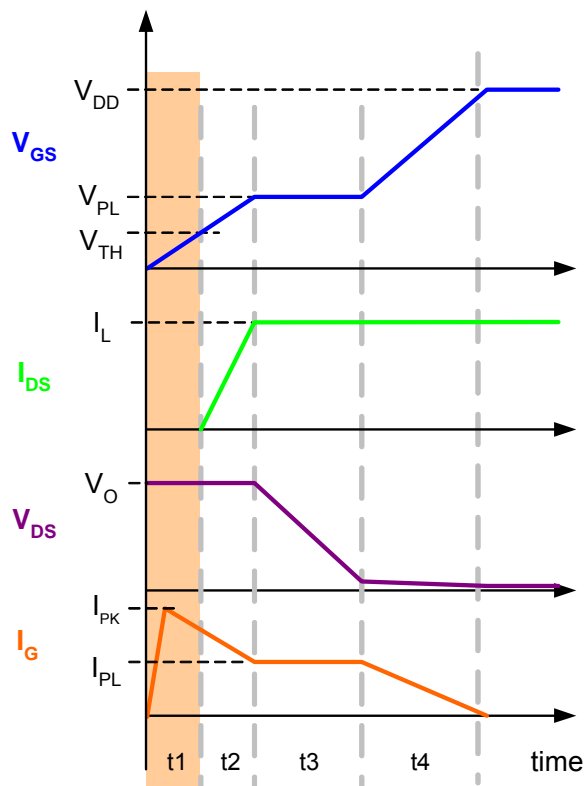
- Direct low-side driver in PWM controller
  - PWM output in low to mid power applications (100 to 200W)
  - Flyback, boost, forward applications
- When is PWM onboard driver acceptable?
  - MOSFET switching times provide acceptable efficiency
  - Control circuit not disrupted by noise
  - Heat dissipation is within acceptable limits
- When are external drivers needed?
  - Higher power requires more current capability
  - Need translation from logic levels to higher gate drive voltage
  - IGBTs need high voltage drive (>15V)
  - Grounding, noise and heat issues affect operation
  - Application requires driving gate or pulse transformers

# Examine Boost with Clamped Inductive Load



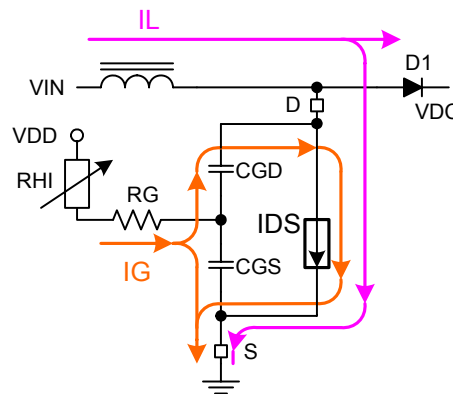
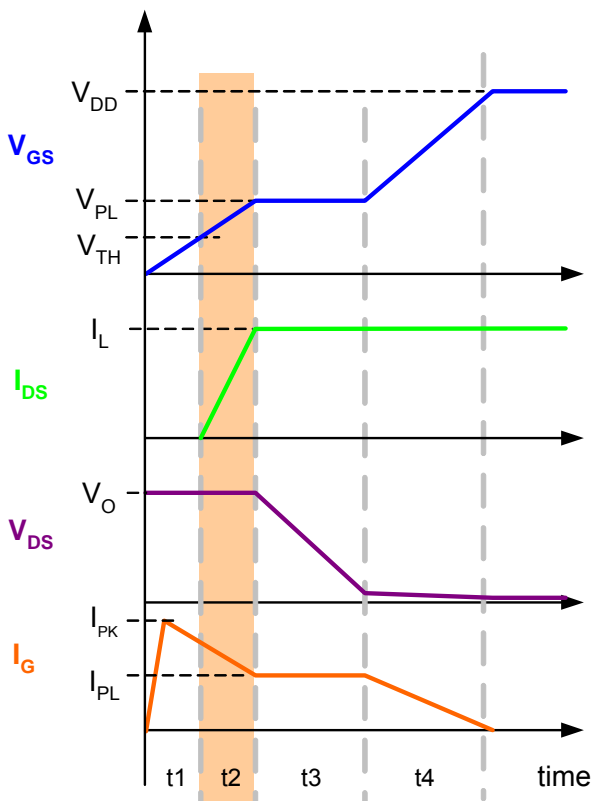
- Non-isolated boost stage
- Illustrates clamped inductive load switching
- Inductor L is large, constant current during switching intervals
- Switching intervals are examined in following slides as in [1], [2]
- Allow user to estimate  $I_G$  requirements

# MOSFET Turn on in Interval t1



- Initially MOSFET is off,  $V_{DS} = V_{OUT}$
- $I_G$  charges  $C_{GS} \parallel C_{GD}$  to  $V_{TH}$
- $I_G$  amplitude is limited by
  - driver output current capability
  - external resistance
  - parasitic inductance

# MOSFET Turn on Interval t2



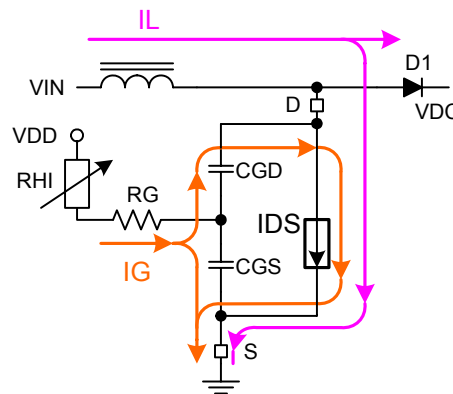
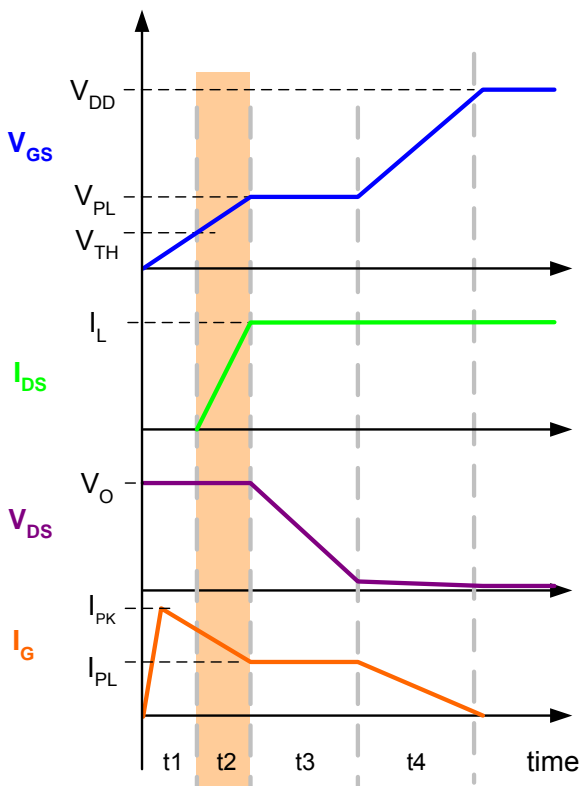
- $V_{TH}$  is exceeded and MOSFET starts conducting in linear mode:

$$I_D = g_m (V_{gs} - V_{TH})$$

- $I_{DS}$  rises in MOSFET channel from 0 to  $I_L$
- During  $t_2$   $C_{GD}$  and  $C_{GS}$  are charged to a level:

$$V_{PL} = \frac{I_L}{g_m} + V_{TH}$$

# What is the Length of Interval t2?

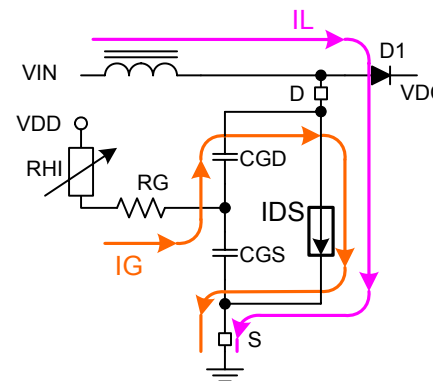
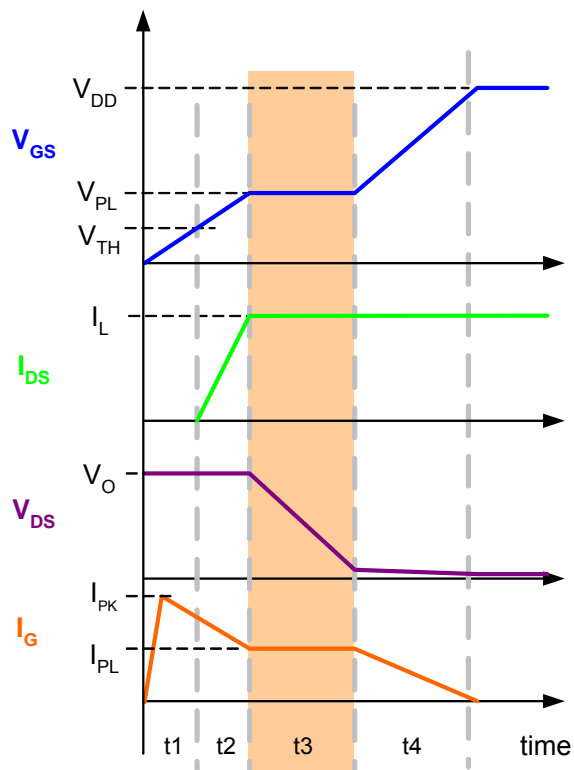


- $I_{DS}$  rises in MOSFET channel from 0 to  $I_L$
- $t_2$  interval length can be defined as

$$t_2 = T_{IDS,rise} = \frac{Q_{gs2}}{I_G}$$

- $Q_{GS2}$  specified by MOSFET datasheet
- $I_G$  is the current delivered during  $t_2$

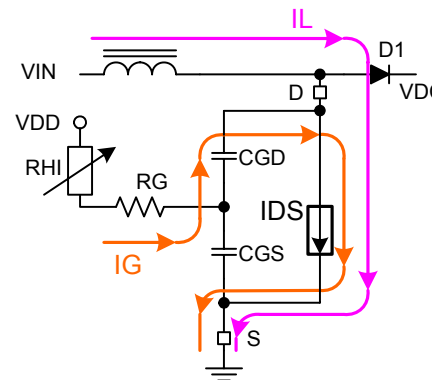
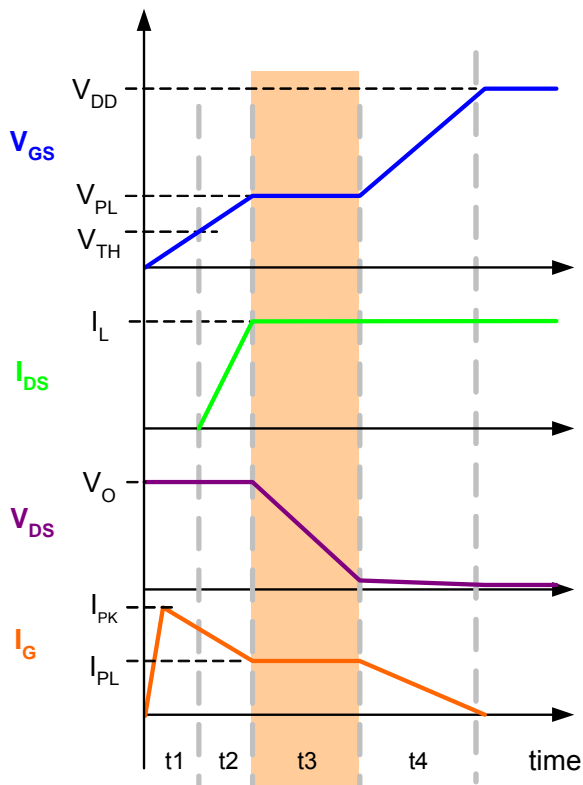
# Interval t3 – Known as “Miller” region



- $I_G$  flows through  $C_{GD}$  while  $V_{GS}$  remains at  $V_{PL}$
- MOSFET conducts full  $I_L$  while  $V_{DS}$  falls from  $V_{DC}$  toward GND
- How can we determine driver current capability (Amps) required?



# What is the Length of Interval t3?

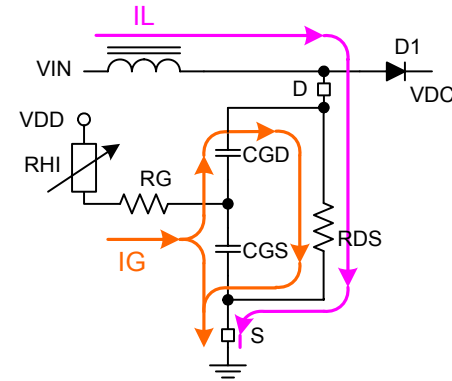
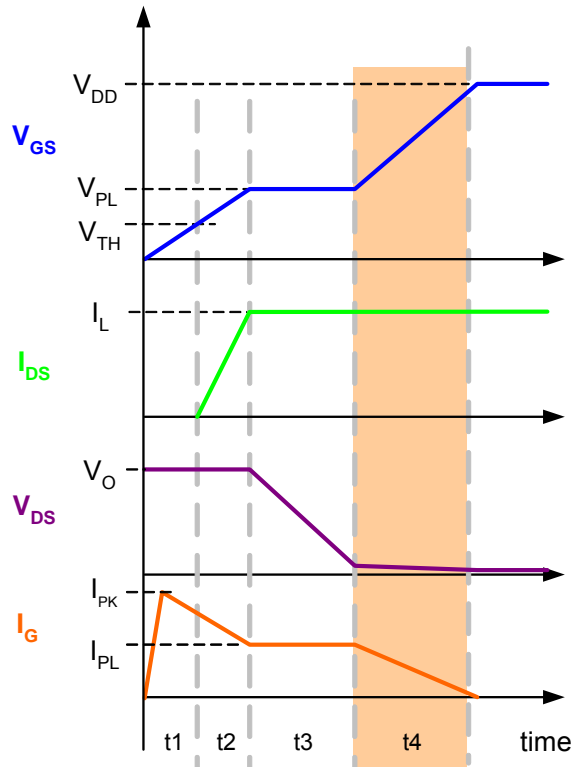


- $t_3$  interval approximated by

$$t_3 = T_{vds,f} = \frac{Q_{GD}}{I_G}$$

- $Q_{GD}$  derived from MOSFET datasheet
- $I_G$  is a function of
  - driver current source capability
  - external impedances

# MOSFET Turn on Interval $t_4$

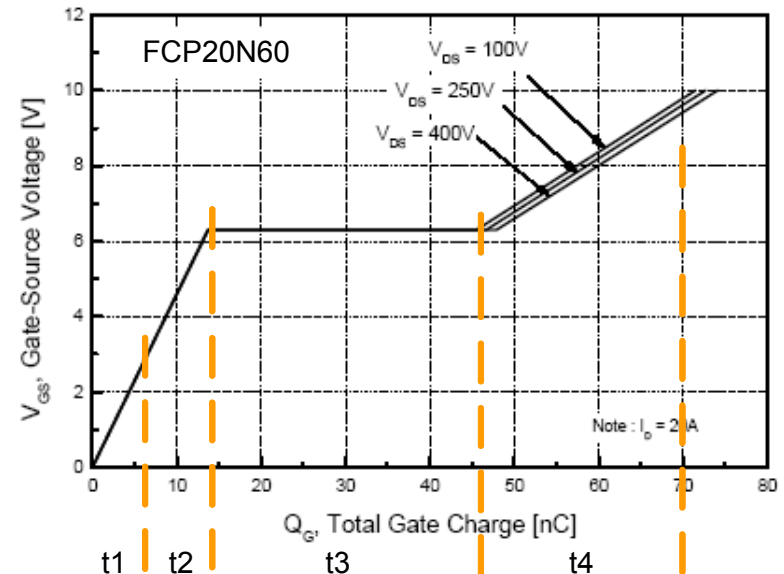


- $V_{GS}$  rises from  $V_{PL}$  to  $V_{DD}$
- $I_G$  charges  $C_{GD} || C_{GS}$
- $R_{DS}$  reaches low value

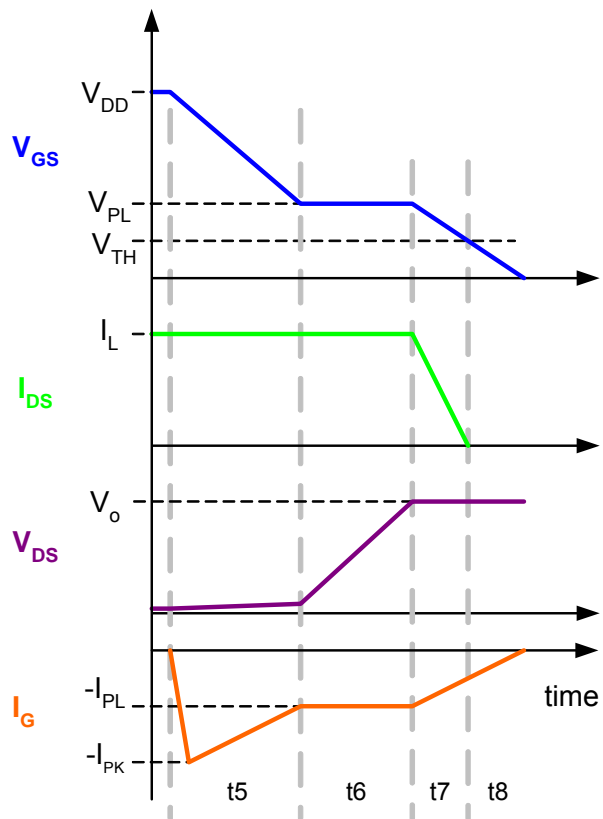
## Equate Intervals to Datasheet Gate Charge Curve

- t1 –  $V_{GS}$  reaches  $V_{TH}$  (3V)
- t2 –  $V_{GS}$  reaches  $V_{PL}$  (6.2V)
- t3 –  $Q_{GD}$  delivered as  $V_{DS}$  swings low (32 nC)
- t4 –  $V_{GS}$  enhanced to 9.5V with  $Q_{G,T} = 70$  nC
- Average current from  $V_{DD}$  is  

$$I_{DD} = Q_G \times f_{SW}$$

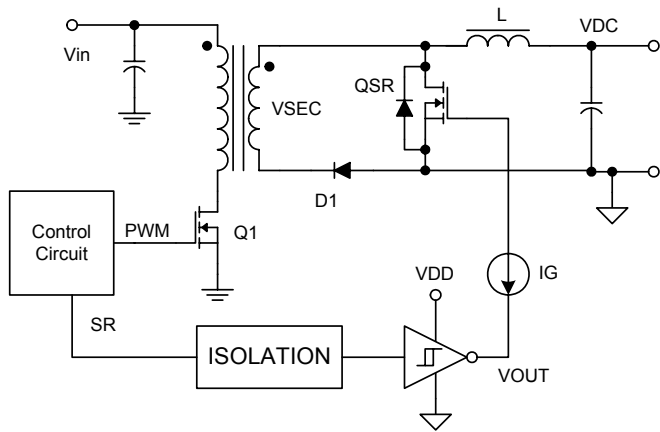


# Boost Turn off waveforms

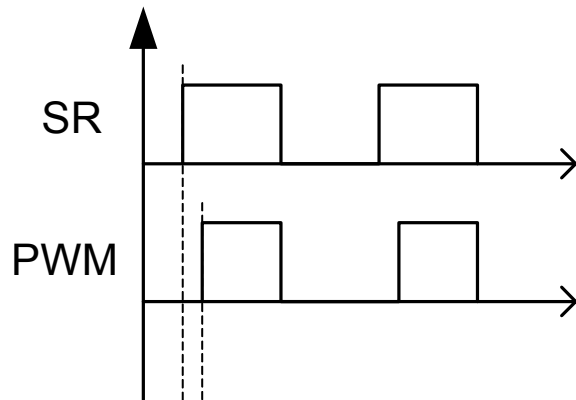


- Turn off proceeds in reverse order from turn on
- $t_5$  –  $V_{GS}$  discharges to  $V_{PL}$
- $t_6$  –  $I_G$  constant as  $V_{DS}$  rises
- $t_7$  –  $V_{GS}$  decrease reduces  $I_{DS}$
- $t_8$  –  $V_{GS}$  is discharged to 0V

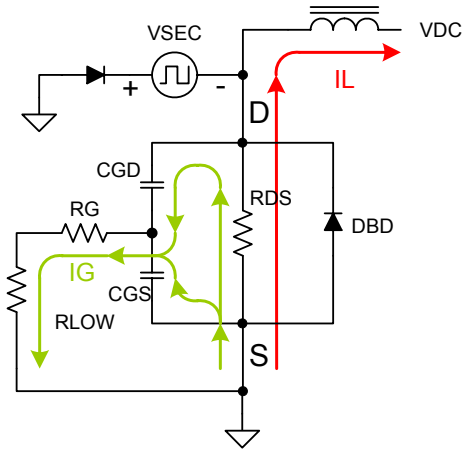
## Forward Converter with Secondary Sync. Rectifier



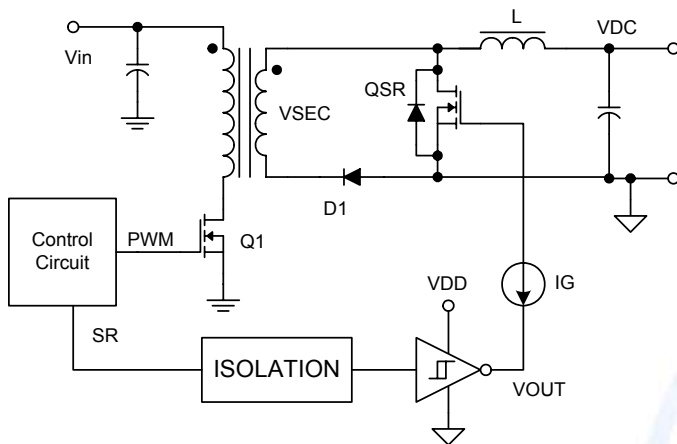
- Simplified forward converter with freewheel diode replaced by  $Q_{SR}$
- $Q_{SR}$  conducts when  $Q1$  is off
- $Q_{SR}$  must turn off before  $Q1$  turns on
- SR signal leads PWM as indicated
- SR signal generation
  - primary controller
  - external timing circuitry



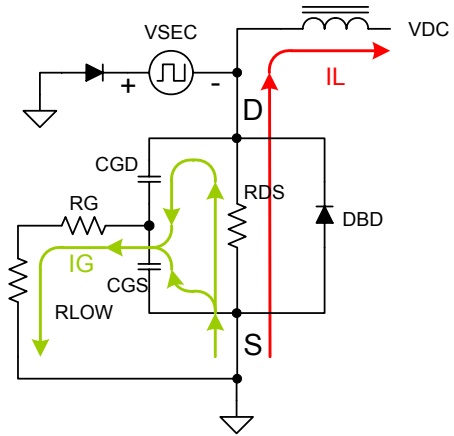
# SR MOSFET Turn off operation



- Initially, inductor current flows through MOSFET channel  $R_{DS}$
- Driver output goes low and sinks current  $I_G$  shown
- In many applications there is no external resistor between driver and MOSFET
- How can we determine driver current capability (Amps) required?



# What Driver is Needed for SR MOSFET?



- Turn-off time can be estimated using  $Q_{Q,SR}$  as determined in [3]

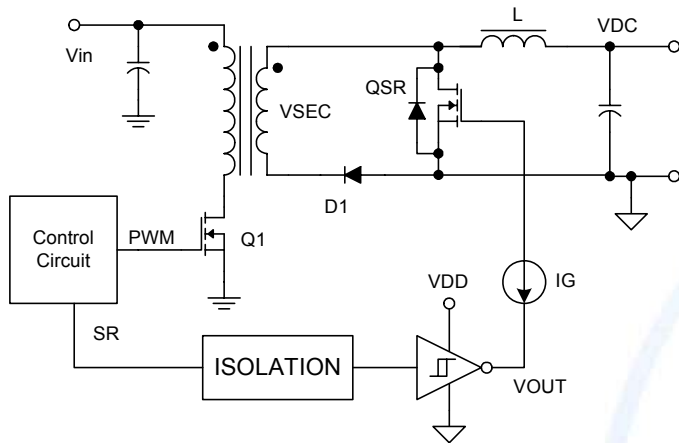
$$t_{off} = \frac{Q_{Q,SR}}{I_G}$$

- With  $Q_{Q,SR} = (C_{GS} + C_{GD,SR}) \cdot V_{DRV}$

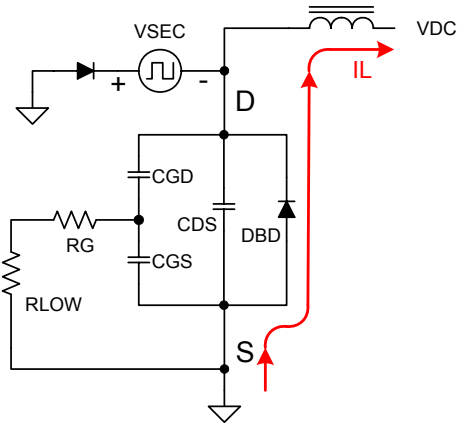
$$C_{GD,SR} = 2 \cdot C_{RSS,SPEC} \cdot \sqrt{\frac{V_{DS,SPEC}}{0.5 \cdot V_{DRV}}}$$

$$C_{GS} = C_{ISS} - C_{RSS}$$

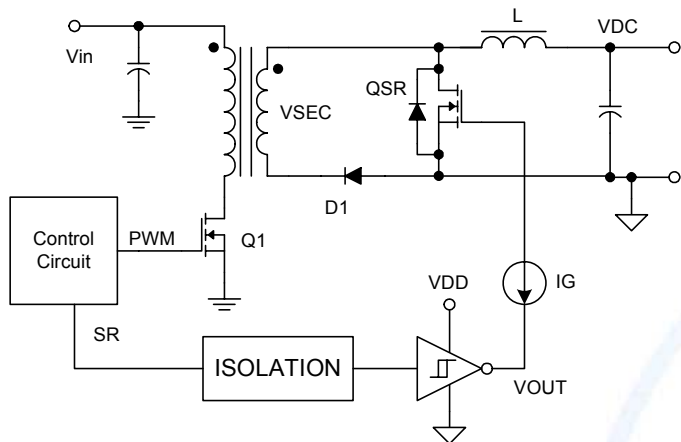
- $C_{ISS}$  and  $C_{RSS}$  found on datasheet curves,  $C_{GS}$  approximately constant
- What value should be used for  $I_G$ ?



# SR MOSFET with $V_{gs} = 0$

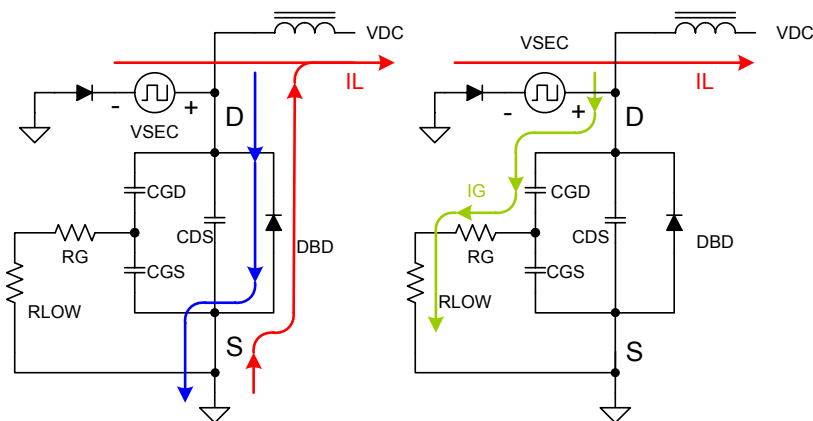


- With MOSFET OFF,  $I_L$  flows through body diode  $D_{BD}$
- This current flow is determined by external circuit, not MOSFET gate-source voltage
- No gate current flows

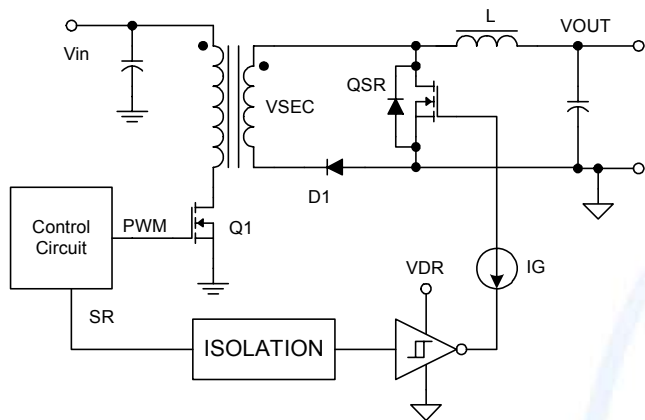




# SR MOSFET dV/dT interval



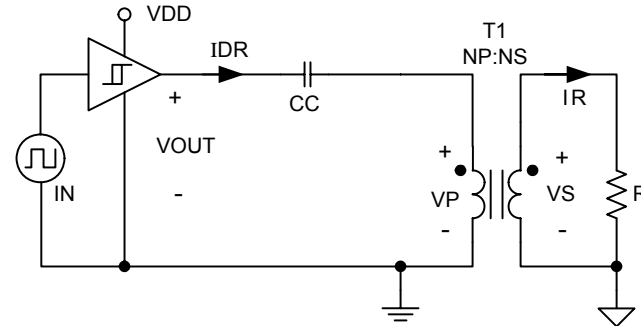
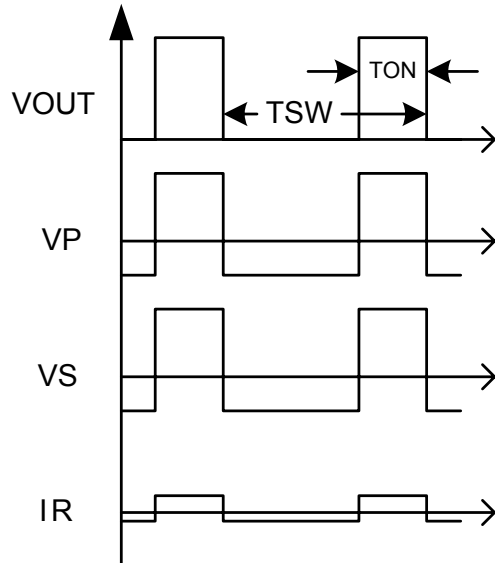
- $V_{SEc}$  polarity switches as shown with  $V_{SEc}$  (-) clamped by diode
- This forces reverse recovery current (blue) through body diode and  $I_L$  transfers to  $V_{SEc}$  (left)
- After  $D_{BD}$  recovers  $V_{DS}$  rises
- With no current in  $C_{GS}$ , driver sinks current (right)



$$I_G = C_{GD} \cdot \left( \frac{dV_{DS}}{dT} \right)$$

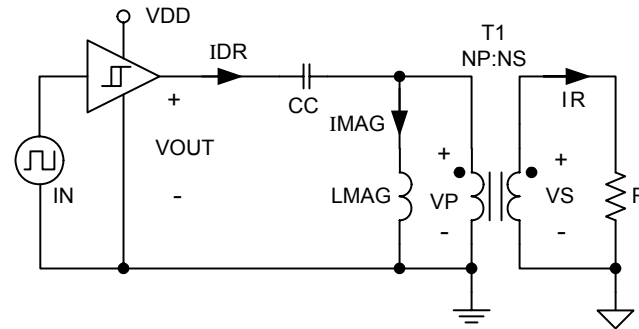
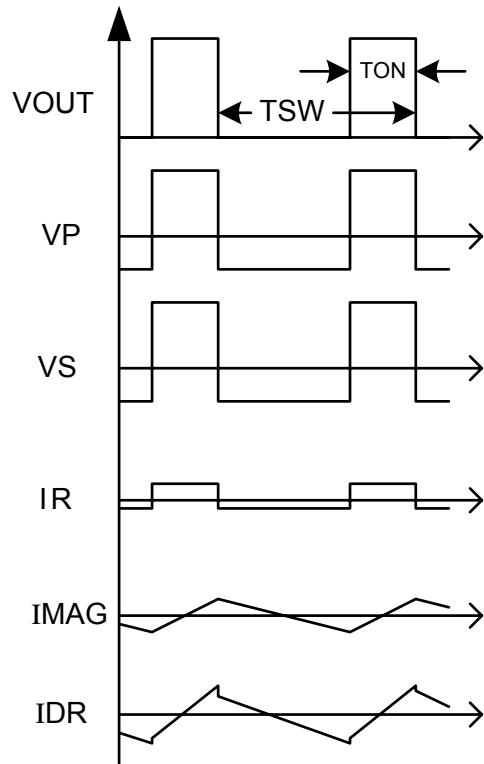
- Gate drive transformer applications
  - Higher power converters often have high/low switches
  - High voltage or primary-secondary isolation may be needed
  - Short propagation delays resulting from small leakage inductance improves protection [4]
  - Competition: half-bridge gate drive ICs
- Pulse transformers used for communication
  - communication needed for enhanced performance
  - competition: high speed opto-isolators with digital outputs
- These two applications can look similar

# Pulse Transformer With Resistive Load



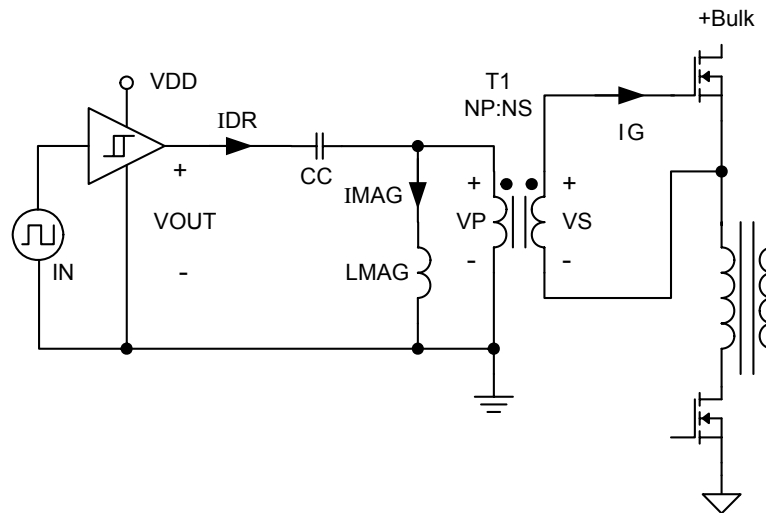
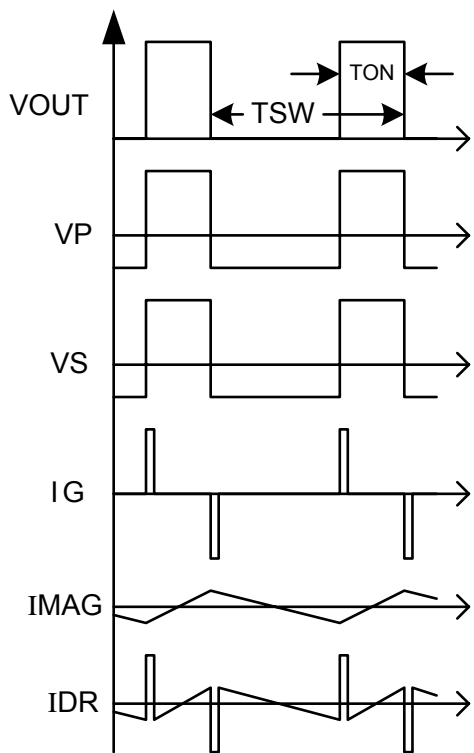
- V<sub>OUT</sub> has DC voltage component
- Transformer cannot support DC voltage
- C<sub>C</sub> blocks DC voltage but passes AC
- C<sub>C</sub> selected with ripple voltage  $\ll V_{OUT}$  while passing I<sub>DR</sub>
- With N<sub>p</sub>=N<sub>s</sub>, V<sub>P</sub> and V<sub>S</sub> are centered at 0V and amplitudes change with duty cycle
- Positive Volt-sec = negative Volt-sec

# Pulse Transformer With Resistive Load-2



- Transformer is replaced by magnetizing inductance in parallel with ideal transformer
- $I_{DR}$  is equal to magnetizing current  $I_{MAG}$  plus reflected resistive current  $I_R$
- $I_{MAG}$  is defined by  $L_{MAG}$ , voltage, and time (not load)

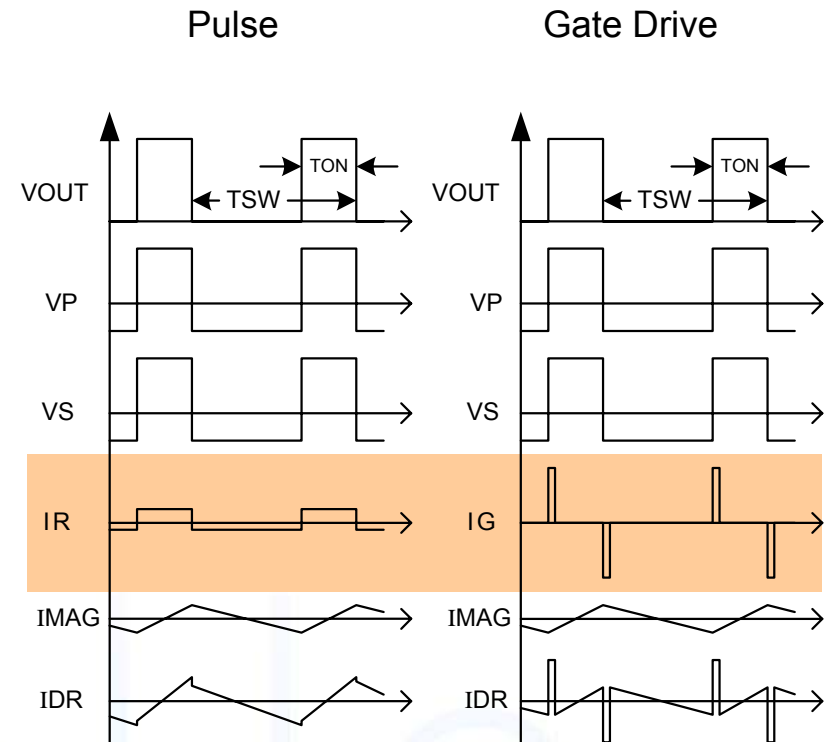
# Change to MOSFET Gate Drive Application



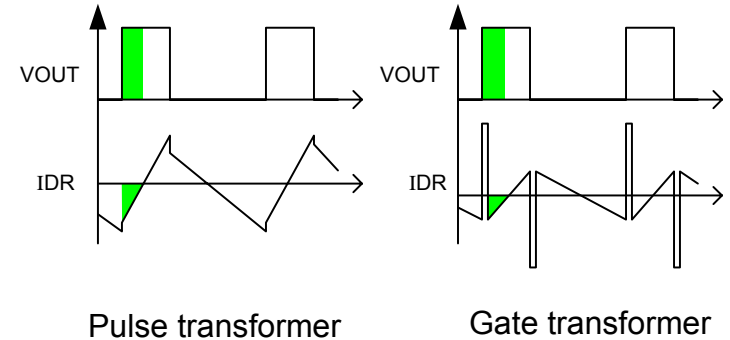
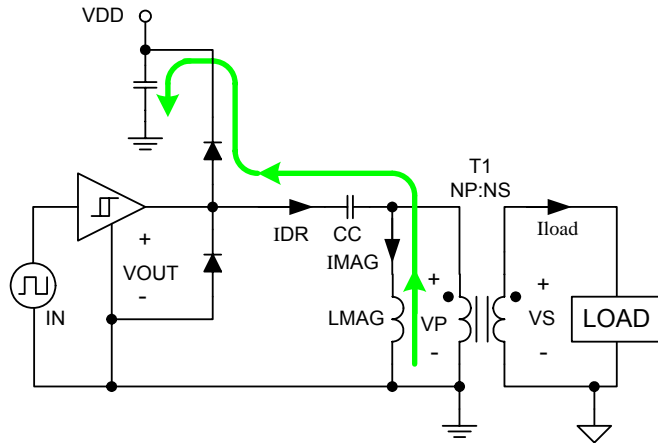
- Exchange R with MOSFET on high side in bridge circuit
- $I_{DR}$  is a combination of pulses to switch MOSFET  $I_G$  and magnetizing current  $I_{MAG}$
- Driver must supply  $I_G$  pulses for acceptable switching operation

# Comparison of Pulse to Gate Drive operation

- For these applications  $V_{OUT}$ ,  $V_P$ ,  $V_S$ , and  $I_{MAG}$  are the same
- $I_R$  and  $I_G$  are very different
- Winding DC resistance (DCR) should be checked for voltage drop and losses
- Same transformer often works in either circuit
- Transformer E-T Product (V-us) calculated on secondary side

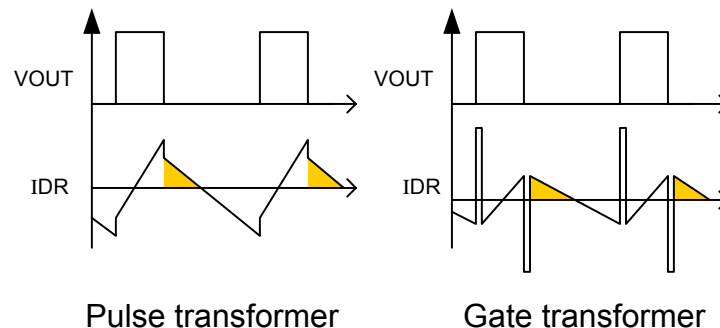
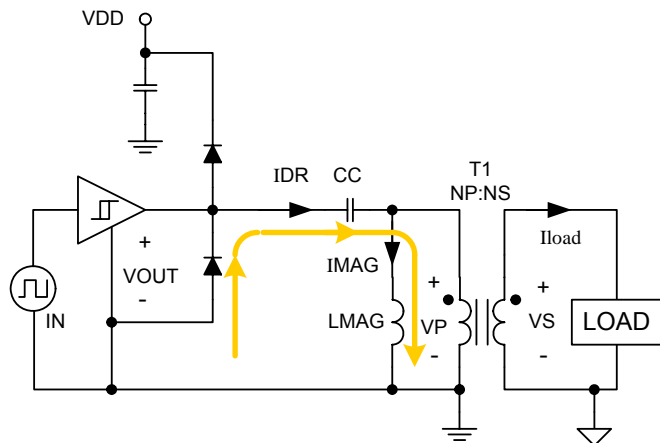


# Driver Reverse Current - $V_{OUT}$ High



- Before  $V_{OUT}$  goes HIGH,  $I_{MAG}$  is negative and driver sinks current
- When  $V_{OUT}$  goes HIGH driver must continue to sink current
- Bipolar drivers need external diodes, MOSFET drivers can conduct reverse current through channel, body diode

# Driver Reverse Current Vout - Low



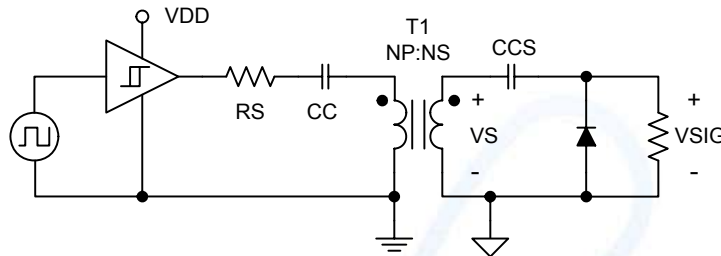
- Before  $V_{OUT}$  goes LOW,  $I_{MAG}$  is positive and driver sources current
- When  $V_{OUT}$  goes LOW driver must continue to source current
- Bipolar drivers need external diodes, MOSFET drivers can conduct reverse current through channel, body diode



# Modified Pulse Transformer Circuit

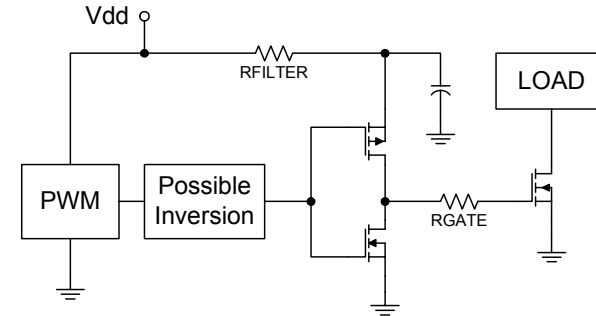
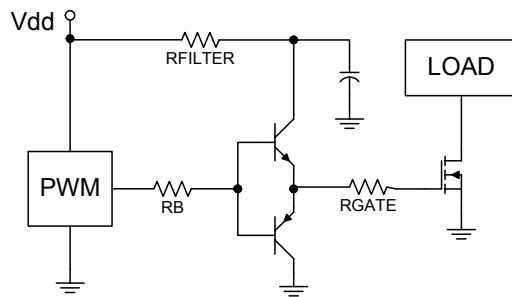
- In initial pulse transformer circuit  $V_S$  is related to  $V_{DD}$  by turns ratio, and varies with duty cycle
- $C_{CS}$  and D clamp  $V_{SIG}$  with GND reference
- $C_C$  and  $L_{MAG}$  undergo startup transient
- Series  $R_S$  can be selected to provide critical damping

$$R_S = 2 \cdot \sqrt{\frac{L_{MAG}}{C_C}}$$



- Discrete designs built from bipolar or MOSFET devices
- Integrated circuit devices using bipolar, MOSFET, or compound (combined) device technologies
- All driver applications benefit from:
  - Local bypass capacitor
  - filtering from control circuit Vdd
  - location close to load
  - capability to dissipate power

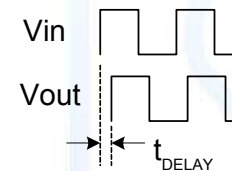
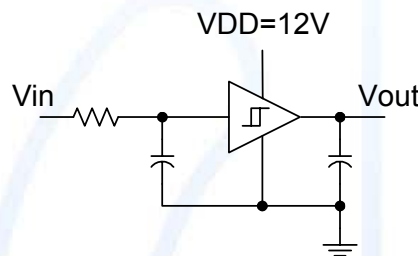
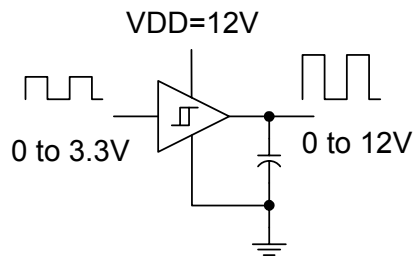
# Discrete Driver Configurations



- NPN/PNP emitter follower
  - Non-inverting configuration works directly in phase with control chip
  - No shoot-thru, devices not on simultaneously
  - Output has no ohmic connection to rails
- PMOS/NMOS driver (inverter)
  - Natural inversion requires additional inversion to follow control
  - Overlap in  $V_{GS}$  conduction range leads to shoot-thru
  - Rail to rail operation

- More individual devices needed in circuit
  - assembly and test time grow
  - more reliability concerns
- Translation from logic level inputs to higher voltage drive levels adds complexity
- For fast switching, input driving signal needs fast edges (output not fully buffered from input)
- Difficult to introducing delay through drive stage while keeping fast edge rates
- MOS shoot-thru power loss increases with frequency

- Integrated features can reduce supporting circuitry
  - enable functions can simplify control in SR applications
  - UVLO can provide orderly startup in secondary side circuits
- Facilitates direct translation from TTL inputs to higher  $V_{GS}$
- High impedance inputs with CMOS thresholds facilitate programming time delay in driver (HIGH =  $2/3 V_{DD}$ , LOW =  $1/3 V_{DD}$ )
- Device input current usually negligible
- Small MLP packages enable highest density designs
  - dual 2 A, 4 A drivers in 3x3 mm ; single 2 A in 2x2 mm
  - thermal pads allow reduced thermal impedance
- Summary: Less component level design required from users

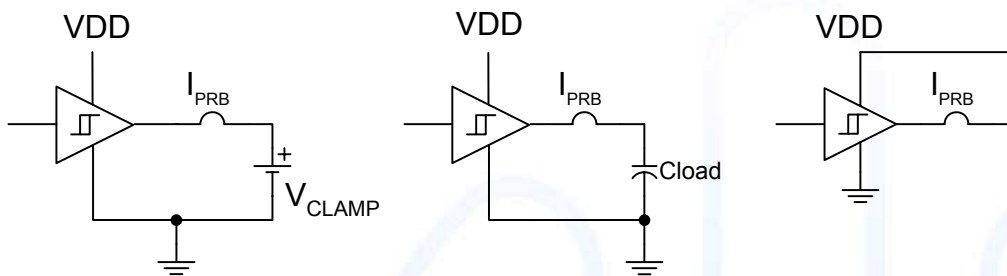


# How Ideal are Real Drivers?

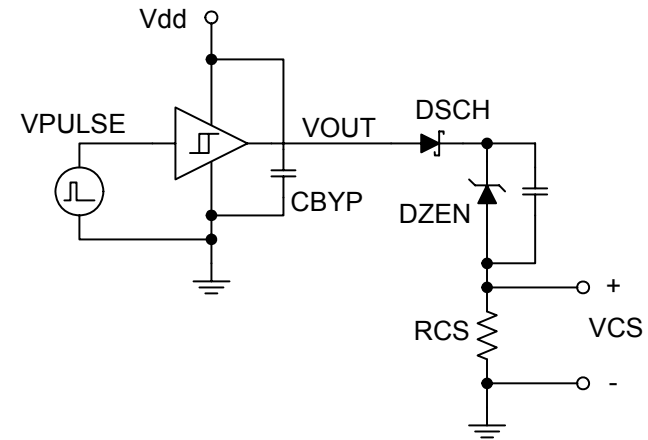
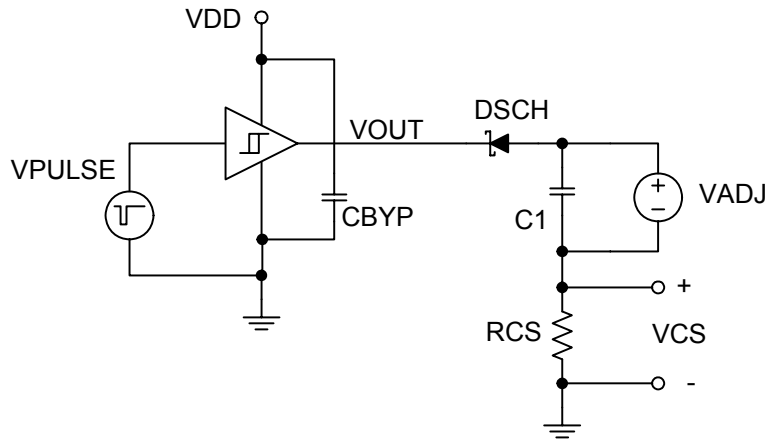
- Many users treat drivers as near-ideal signal amplifiers
- Some assumptions may not be justified:
  - Sink and source current defined by series resistances
  - Output slew rates are instantaneous
- Output current varies with  $V_{DD}$ , parasitic impedances, size of external load, temperature, other factors
- Output rise/fall specifications don't give much insight into instantaneous current capability

# How do Driver Datasheets Rate Current?

- Current specified in one of several ways
  - Peak current available from driver
  - Current available with output at clamped voltage level
  - Current available through low value resistance (or short circuit)
  - Measure current with current probe – bandwidth, inductance concerns
- All driver measurements require attention to detail!



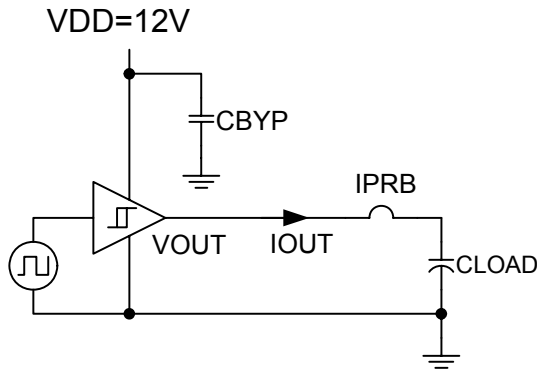
# Clamped Circuits for Pulsed Testing



- These circuits test current capability for pulses of 200ns with **minimal** external resistance ( $R_{CS}$  is 0.05  $\Omega$ )
- With good layout, transient dies out < 100ns
- $V_{PULSE}$  is 200ns pulse at low duty cycle, 2%
- At left –  $I_{SINK}$  is monitored as  $V_{CS}$  goes negative
- On right –  $I_{SOURCE}$  is monitored as  $V_{CS}$  is positive

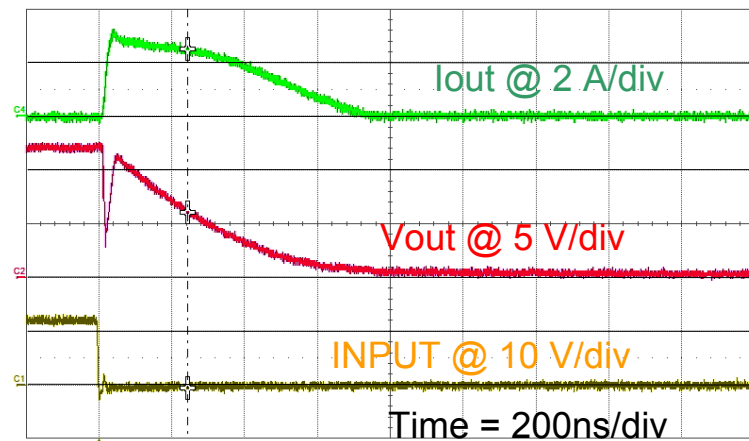
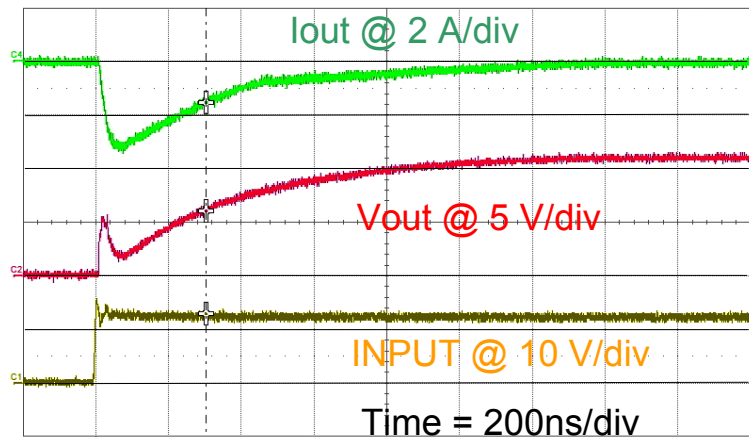


# Driver Testing Using Large Loads



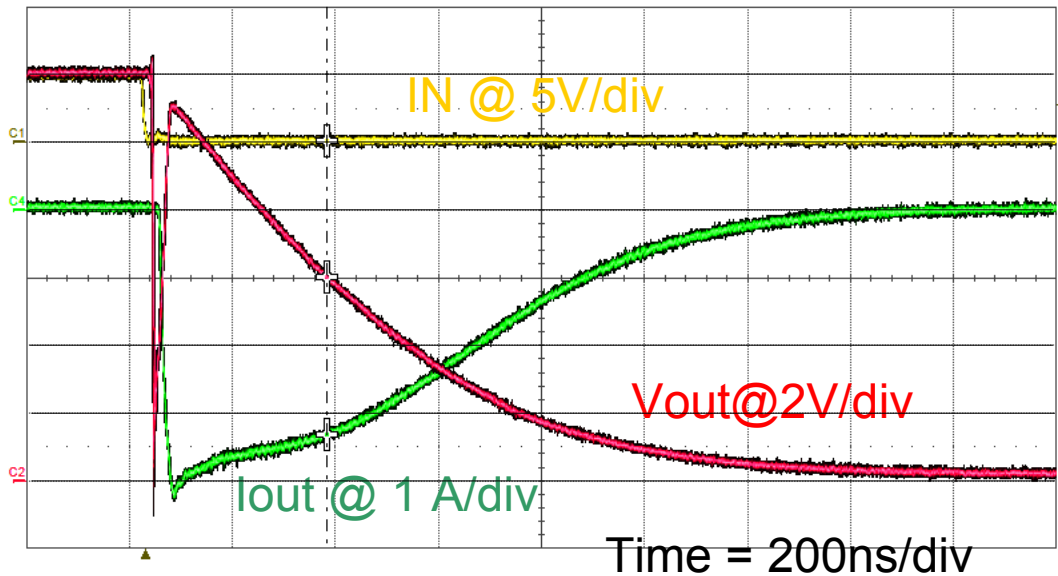
- $I_{PRB}$  monitors  $I_{OUT}$  charging or discharging a large capacitor
- $C_{LOAD}$  chosen as 100x capacitor used in rise/fall time specs
  - 2 Amp –  $100 \times 1\text{nF} = 0.1\mu\text{F}$
  - 4 Amp –  $100 \times 2.2\text{nF} = 0.22\mu\text{F}$
- This allows measurement of  $I_{OUT}$  at various values of  $V_{OUT}$
- This is maximum current available from driver with **NO** external resistance
- This equates to the pulse current values obtained in clamped sink and source circuits

# Look at 2 Amp Drivers with Large Load

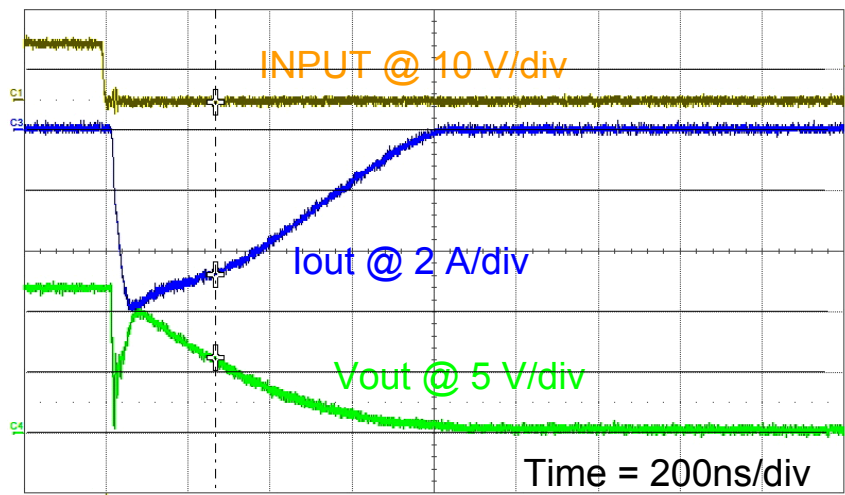
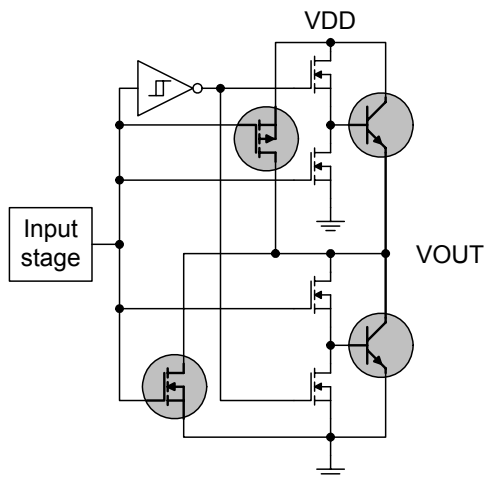


- Note initial transient due to current loop inductance (<100ns)

- MOS-based drivers spec peak current and  $R_{DS,high}$  or  $R_{DS,low}$
- The  $R_{DS,on}$  values not achieved during early stages of turn on
- Peak current is significantly less than  $I=V_{DD}/R_{DS}$
- In examples tested, datasheet current rating is peak current available from device

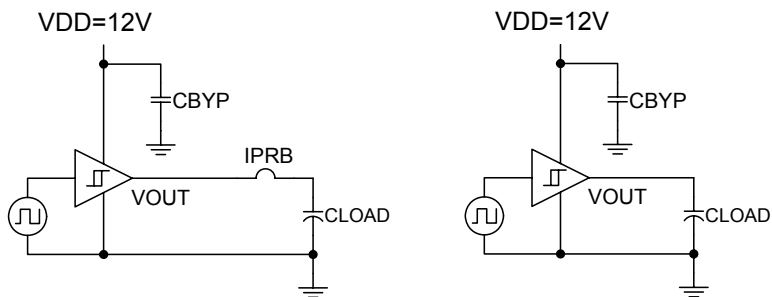


# Integrated Driver with Compound Output Stage

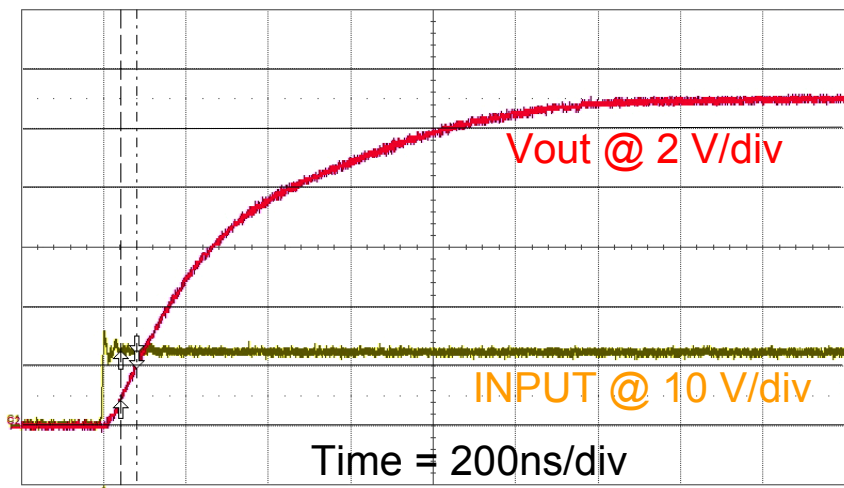


- Compound output stage combines bipolar and MOSFET
- Bipolars provide current during mid range of  $V_{OUT}$  and clamp  $V_{OUT}$  within 1 volt of rails
- MOSFETs pull  $V_{OUT}$  to rails and offers bi-directional current capability
- FAN3224C shows 6 Amp  $I_{SINK,pk}$
- FAN3224C sinks 4.5 Amps at  $V_{OUT} = 6V$  (datasheet says 4 Amp driver)

# Now Remove Current Probe



- $I_{PRB}$  requires wire loop for current probe
- $C_{LOAD}$  is surface mount 0.1uF, (0805) with minimal inductance
- Note lack of initial transient!
- Calculate current from familiar equation applied over short, approximately linear interval.



$$I = C_{LOAD} \cdot \left( \frac{dV_{OUT}}{dT} \right)$$

$$I = 0.1\mu F \cdot \left( \frac{1.131V}{40.6ns} \right) = 2.8A$$

# Summary of Driver Presentation

- Key low-side driver applications include
  - ground referenced switches
  - SR applications
  - pulse and gate drive transformer applications
- Potential drivers include integrated and discrete
  - PMOS-NMOS drivers
  - bipolar drivers
  - compound drivers which combine bipolar and MOSFET
- Lab evaluation of drivers current capability
  - presented progression of pulse and “large load” circuits
  - correlated lab data provide confidence in results

- [1] 2006 Fairchild Power Seminar Topic, “Understanding Modern Power MOSFETs,”  
[http://www.fairchildsemi.com/powerseminar/pdf/understanding\\_modern\\_power\\_mOSFETs.pdf](http://www.fairchildsemi.com/powerseminar/pdf/understanding_modern_power_mOSFETs.pdf)
- [2] Oh, K. S., “MOSFET Basics”, July, 2000, available as AN9010 from the fairchildsemi.com website
- [3] Balogh, L. “Design and Application Guide for High Speed MOSFET Gate Drive Circuits,” Power Supply Design Seminar SEM-1400, Topic 2, Texas Instruments Literature No. SLUP169
- [4] ICE Components Gate Drive Transformer Datasheet “GT03.pdf” dated 10/06, available from [www.icecomponents.com](http://www.icecomponents.com)
- [5] 2006 Fairchild Power Seminar Topic, “Practical Power Application Issues for High Power Systems,”  
[http://www.fairchildsemi.com/powerseminar/pdf/practical\\_power\\_high\\_power\\_systems.pdf](http://www.fairchildsemi.com/powerseminar/pdf/practical_power_high_power_systems.pdf)
- [6] Johnson, H. Dr, “High-Speed Digital Design On-Line Newsletter,” Vol. 3 Issue 8,  
[www.sigcon.com/Pubs/news/3\\_8.htm](http://www.sigcon.com/Pubs/news/3_8.htm)